# PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

## PCT

### NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Assistant Commissioner for Patents
United States Patent and Trademark Office
Box PCT
Washington, D.C.20231
ETATS-UNIS D'AMERIQUE

in its capacity as elected Office

| | |
|---|---|
| **Date of mailing** (day/month/year)<br>13 June 2000 (13.06.00) | |
| **International application No.**<br>PCT/SG98/00086 | **Applicant's or agent's file reference**<br>ST/61772 |
| **International filing date** (day/month/year)<br>26 October 1998 (26.10.98) | **Priority date** (day/month/year) |
| **Applicant**<br>PAI, Pratima et al | |

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

05 May 2000 (05.05.00)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

| | |
|---|---|
| **The International Bureau of WIPO**<br>**34, chemin des Colombettes**<br>**1211 Geneva 20, Switzerland** | Authorized officer<br>S. Mafla |
| Facsimile No.: (41-22) 740.14.35 | Telephone No.: (41-22) 338.83.38 |

PATENT COOPERATION TREATY

# PCT

## INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

| Applicant's or agent's file reference | **FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below. | |
|---|---|---|
| ST/61772 | | |
| International application No. | International filing date *(day/month/year)* | (Earliest) Priority Date *(day/month/year)* |
| PCT/SG 98/ 00086 | 26/10/1998 | |
| Applicant | | |
| STMICROELECTRONICS ASIA PACIFIC PTE LTD et al. | | |

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 2 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 4

   [ ] as suggested by the applicant.

   [X] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [ ] None of the figures.

# INTERNATIONAL SEARCH REPORT

International Application No
PC[redacted]G 98/00086

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F9/445 H04M11/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F H04M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | WILSON HO W ET AL: "AN APPROACH TO GENUINE DYNAMIC LINKING" SOFTWARE PRACTICE & EXPERIENCE, vol. 21, no. 4, 1 April 1991, pages 375-390, XP000147180 | 1-7 |
| Y | see page 380, line 1 - line 40; figure 2 | 6,7 |
| A | EP 0 772 370 A (IBM) 7 May 1997 | 1,3-5 |
| Y | see column 6, line 7 - line 47; figures 2,3 | 6,7 |

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 18 June 1999 | 25/06/1999 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Kingma, Y |

1

Form PCT/ISA/210 (second sheet) (July 1992)

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 98/00086

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| EP 0772370 A | 07-05-1997 | JP 9134320 A | 20-05-1997 |

PATENT COOPERATION TREATY



# PCT

## INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

| Applicant's or agent's file reference | FOR FURTHER ACTION | See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416) |
|---|---|---|
| ST/61772 | | |
| International application No. | International filing date *(day/month/year)* | Priority date *(day/month/year)* |
| PCT/SG98/00086 | 26/10/1998 | 26/10/1998 |
| International Patent Classification (IPC) or national classification and IPC<br>G06F9/445 | | |
| Applicant<br>STMICROELECTRONICS ASIA PACIFIC PTE LTD et al. | | |

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 5 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

| Date of submission of the demand | Date of completion of this report |
|---|---|
| 05/05/2000 | 25.01.2001 |
| Name and mailing address of the international preliminary examining authority:<br>European Patent Office<br>D-80298 Munich<br>Tel. +49 89 2399 - 0 Tx: 523656 epmu d<br>Fax: +49 89 2399 - 4465 | Authorized officer<br>Bauer, R<br>Telephone No. +49 89 2399 7483 |

Form PCT/IPEA/409 (cover sheet) (January 1994)

# INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/SG98/00086

## I. Basis of the report

1. This report has been drawn on the basis of *(substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments (Rules 70.16 and 70.17).)*:
**Description, pages:**

| | | | | |
|---|---|---|---|---|
| 1,5-7 | as originally filed | | | |
| 2-4 | as received on | 24/10/2000 | with letter of | 19/10/2000 |

**Claims, No.:**

| | | | | |
|---|---|---|---|---|
| 1-7 | as received on | 24/10/2000 | with letter of | 19/10/2000 |

**Drawings, sheets:**

| | |
|---|---|
| 1/2,2/2 | as originally filed |

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   - ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
   - ☐ the language of publication of the international application (under Rule 48.3(b)).
   - ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   - ☐ contained in the international application in written form.
   - ☐ filed together with the international application in computer readable form.
   - ☐ furnished subsequently to this Authority in written form.
   - ☐ furnished subsequently to this Authority in computer readable form.
   - ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   - ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

   *(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)*

6. Additional observations, if necessary:

**V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

| | | |
|---|---|---|
| Novelty (N) | Yes: | Claims 1-7 |
| | No: | Claims |
| Inventive step (IS) | Yes: | Claims 2 |
| | No: | Claims 1,3-7 |
| Industrial applicability (IA) | Yes: | Claims 1-7 |
| | No: | Claims |

2. Citations and explanations
   **see separate sheet**

**VII. Certain defects in the international application**

The following defects in the form or contents of the international application have been noted:
**see separate sheet**

**VIII. Certain observations on the international application**

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
**see separate sheet**

**Re Item V**

**Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Claim 1 is new (Art. 33.2) PCT) . However the subject-matter of claim 1 is not inventive (Art. 33.3) PCT), because it does not recite elements that would lead to solve the technical problem stated by the Applicant.

   Claim 1 lacks the essential step of overwriting a previously down loaded segment with a newly down loaded segment, which is the step which leads to a reduction of the on-chip RAM requirements.
   The mere fact to download programs segments successively between periods of inactivity of a data transfer function does not solve any technical problem, nor does it bring any technical advantage.

   The Applicant should have amended claim 1 so that it would have encompassed all elements needed in order to solve that technical problem.

2. The subject-matter of claim 1 is not inventive, but the subject-matter of claim 2 is.

3. Claims 4,5,6,7 are only inventive when they would be taken in combination with the features known from claim 2.
   When their subject-matter is taken in combination with claim 1, those combinations lack an inventive step. Hence this report mentions that their subject-matter lacks inventiveness.

**Re Item VII**

**Certain defects in the international application**

4. The features of the claims are not provided with reference signs placed in parentheses (Rule 6.2(b) PCT).
   Further, the last paragraph of the description (p 7) is not clear because it is not clear what "spirit of the invention" means. It should have been amended,.

**Re Item VIII**

**Certain observations on the international application**

5. The description describes only an embodiment involving a modem architecture, and points out that the requirements for the invention to achieve an effect are that the transmission function has inactivity intervals, and also that the time spent for down loading the instructions is substantially smaller than the inactivity interval of the transmission function (pages 6-7 of the description).
Hence, the scope of method claim 1 is so broad that it is no longer supported by the description (Art. 6 PCT, Guidelines C-III 6.1). That method claim should have been restricted to modems.

6. In order to ensure the achievement of the disclosed technical effect, namely the fact that on-chip RAM requirements are reduced, every independent claim should have claimed that a segment overwrites a previously down loaded segment.

DSP based systems perform numerical operations on data and are optimised for such operations. A bottleneck in extracting the maximum performance is the limitation imposed by access times to memory. This is usually circumvented by providing on-chip RAM/ROM to supplement the basic DSP core. ROM based solutions preclude upgradability. Downloadable Modem architectures employ on-chip RAM for easy upgradability. This on-chip RAM is expensive compared to slower external memories like SDRAM, Flash etc.

A typical Datapump function has significant internal memory requirements. A straightforward implementation leads to an expensive single chip solution for Downloadable Modem architectures. This implies a large on-chip RAM requirement if all the program code corresponding to the Handshake and Data phase of the Modulation function were loaded in on-chip RAM.

An alternative is to provide program code for the Modulation function in external RAM, in order to free up on-chip memory and minimise costs for a single chip DSP. Figure 1 is an example of such an architecture, as used in current Modem application systems. The DSP 1 performs the Datapump function. The program code for the specific Modulation function used during a modem connection exists in external RAM 2. A slow external memory 3 stores the program code for the whole modem application. This slow external memory 3 is usually a FLASH memory, and is provided as a feature for code-version upgradability. Depending on the Modulation function used, the program code for the Datapump function is loaded into external RAM 2. The memory requirements of this Modulation function code is high because the entire code corresponding to this function is loaded. A significant problem associated with the architecture of Figure 1 is that execution of the modulation function is slowed, as compared to an on-chip DSP RAM architecture, due to the external RAM being generally slower and interfacing delays between the DSP chip and the external RAM. The present invention seeks to maximise efficiency of the DSP operation by utilizing timing constraints of operations performed by the DSP.

An example of dynamically loading or unloading tasks into instruction RAM is disclosed in EP 0 772 370. However that reference makes no mention of any timing constraints for the downloading operations performed by the DSP manager. That is likely because the downloading scheme does not require it. The ability of the DSP manager to allocate space in the data RAM in response to a request from a DSP task does not necessarily imply that inactivity timing constraints are utilized. This is because allocating space in data RAM is different from a downloading operation, it does not involve the transfer of program code from the external PC RAM to the DSP RAM.

OBJECT OF THE INVENTION

It is an object of the invention to provide an architecture and data transfer method to reduce on-chip RAM requirements in a DSP particularly, but not exclusively, in a modem whilst maintaining efficiency.

SUMMARY OF THE INVENTION

In one broad aspect of the invention, there is provided a method of data transfer for use with a signal processor of a modem, including: establishing a program code for executing a data transfer function, the function being divided into phases by inactivity intervals, and the program code including code segments associated with each phase; and downloading each code segment to a memory of the processor prior to commencement of the respective phase for execution thereof, characterised in that: each code segment is downloaded only during the associated inactivity interval.

Preferably, each successively downloaded segment overwrites a previously downloaded segment.

In another aspect, there is provided a modem architecture including: a signal processor with a first internal memory; a second memory external of the signal processor, wherein the second memory is arranged to hold a program code divided into code segments, for executing phases of a modulation function with inactivity intervals therebetween and the first memory is configured to sequentially receive the segments downloaded from the

second memory to a current segment portion of the first memory for executing same; characterised in that the modem architecture is programmed to perform the method steps, as described above.

Preferably, the signal processor is a Datapump and the first memory is provided as on-chip RAM of the Datapump.

In a more particular embodiment of the invention a Downloadable architecture is proposed which subdivides the Modulation function into phases separated by inactivity intervals. The program code segments corresponding to these phases are dynamically downloaded to on-chip RAM during the inactivity intervals without affecting the performance of the modem.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention is more fully described, by way of non-limiting example only, with reference to the accompanying drawings, in which:

Figure 1 is a diagrammatic representation of a prior art Modem Datapump implementation;

Figure 2 is a diagrammatic representation of a subdivision of a Modulation Function into phases;

Figure 3 is an exemplary diagram of a single chip DSP downloadable architecture, in accordance with the invention; and

Figure 4 is a detailed diagram of the single chip DSP downloadable architecture of Figure 3.

## DETAILED DESCRIPTION OF AN EMBODIMENT OF THE INVENTION

The invention utilises a Modulation function which is subdivided into different phases as shown in Figure 2. These phases are subdivided such that there is an inactivity interval between them. Figure 2 shows the typical phases through which a Modulation function passes

THE CLAIMS:

1. A method of data transfer for use with a signal processor of a modem, including: establishing a program code for executing a data transfer function, the function being divided into phases by inactivity intervals, and the program code including code segments associated with each phase; and downloading each code segment to a memory of the processor prior to commencement of the respective phase for execution thereof, characterised in that: each code segment is downloaded only during the associated inactivity interval.

2. A method as claimed in claim 1, wherein each successively downloaded segment overwrites a previously downloaded segment.

3. A method as claimed in claim 1 or 2, wherein the data transfer function is a modem modulation function.

4. A method as claimed in any one of claims 1 to 3, wherein the program code is held in a second memory, external of the signal processor.

5. A method as claimed in any one of claims 1 to 4, wherein the signal processor is in the form of a Datapump.

6. A modem architecture including: a signal processor with a first internal memory; a second memory external of the signal processor, wherein the second memory is arranged to hold a program code divided into code segments, for executing phases of a modulation function with inactivity intervals therebetween and the first memory is configured to sequentially receive the segments downloaded from the second memory to a current segment portion of the first memory for executing same;

characterised in that the modem architecture is programmed to perform the method steps of any one of claims 1 to 5.

7. A modem architecture as claimed in claim 6, wherein the signal processor is a Datapump and the first memory is provided as on-chip RAM of the Datapump.

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
G06F 9/445, H04M 11/06

A1

(11) International Publication Number: WO 00/25206

(43) International Publication Date: 4 May 2000 (04.05.00)

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(22) International Filing Date: 26 October 1998 (26.10.98)

(71) Applicant *(for all designated States except US)*: STMICRO-ELECTRONICS ASIA PACIFIC PTE LTD. [SG/SG]; 28 Ang Mo Kio Industrial Park 2, Singapore 569508 (SG).

(72) Inventors; and

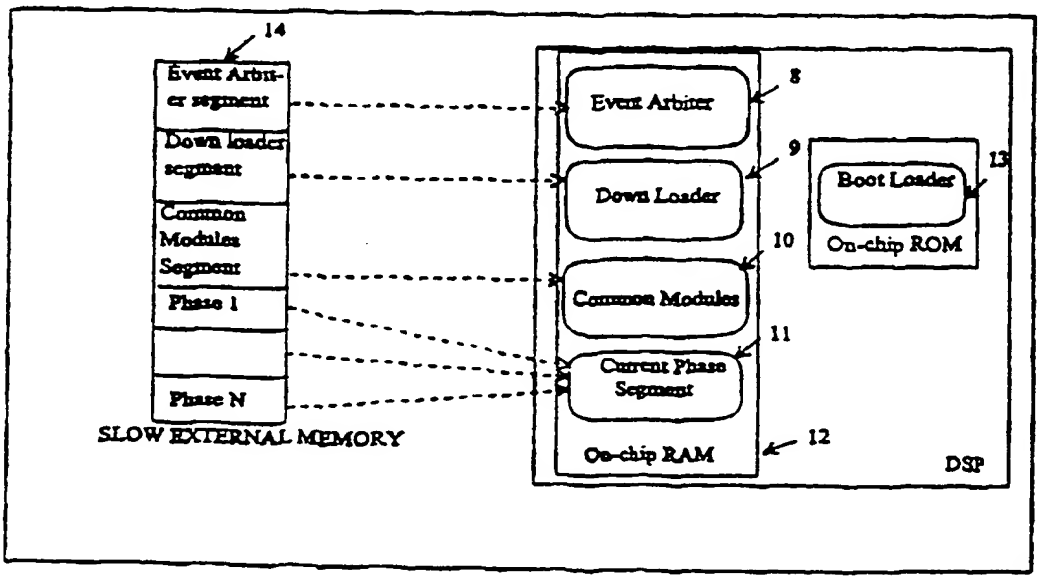
(75) Inventors/Applicants *(for US only)*: PAI, Pratima [IN/SG]; Block 414 Ang Mo Kio Avenue 10, #03–933, Singapore 560414 (SG). DA COSTA, Godfrey [IN/SG]; Block 414 Ang Mo Kio Avenue 10, #03–933, Singapore 560414 (SG). LEONG, Foo, Yuen [SG/SG]; Block 102 Commonwealth Crescent, #10–108, Singapore 140102 (SG).

(74) Agent: DONALDSON & BURKINSHAW; P.O. Box 3667, Singapore 905667 (SG).

(81) Designated States: JP, SG, US, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
*With international search report.*

(54) Title: MODEM ARCHITECTURE AND METHOD OF DATA TRANSFER




(57) Abstract

A modem architecture and a method of reducing on–chip memory requirements in a downloadable modem architecture are provided. The preferred architecture consists of a Digital Signal Processor (DSP) (6) with on–chip Random Access Memory (RAM) (12). A procedure which exploits inactivity intervals in a modem modulation function is provided. The procedure dynamically downloads the requisite code segments for each phase of the function from a cheaper, slower external memory (14) into the DSP on–chip RAM during inactivity intervals, thereby reducing the DSP on–chip RAM requirements.

*FOR THE PURPOSES OF INFORMATION ONLY*

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

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# MODEM ARCHITECTURE AND METHOD OF DATA TRANSFER

## FIELD OF THE INVENTION

The present invention relates to modem architecture and a method of data transfer for reducing on-chip Random Access Memory in a signal processor of a modem.

## BACKGROUND OF THE INVENTION

Typical Modem Architectures consist of a Controller, a Datapump and hardware circuitry also called the Direct Access Arrangement (DAA), to connect to a telephone network. The Controller implements Error Control, Data Compression and digital terminal equipment (DTE) Command/Response interface.

The Datapump is arranged to perform a Datapump function which is usually specified by one of the modem standards ratified by national/international standardisation bodies, which is henceforth referred to as a Modulation function. The specific Datapump function in operation in a modem can be one of a number of Modulation functions. The Modulation functions are usually divided into phases called the Handshake phase and the Data phase. The Handshake phase pertains usually to protocol negotiation (like V.8, V.8bis), channel probing (measurement of channel characteristic), training of modem adaptive elements, and communication of modem parameters. Upon completion of the Handshake Phase, the modem enters the Data phase. These phases are usually separated by inactivity intervals.

The Datapump function (Modulation function in operation) transmits/receives data from a remote modem. The Datapump function usually requires a Digital Signal Processor (DSP) to perform the various numerical operations required for signal generation and reception. Some applications use the DSP power to accommodate the Controller function.

DSP based systems perform numerical operations on data and are optimised for such operations. A bottleneck in extracting the maximum performance is the limitation imposed by access times to memory. This is usually circumvented by providing on-chip RAM/ROM to supplement the basic DSP core. ROM based solutions preclude upgradability. Downloadable Modem architectures employ on-chip RAM for easy upgradability. This on-chip RAM is expensive compared to slower external memories like SDRAM, Flash etc.

A typical Datapump function has significant internal memory requirements. A straightforward implementation leads to an expensive single chip solution for Downloadable Modem architectures. This implies a large on-chip RAM requirement if all the program code corresponding to the Handshake and Data phase of the Modulation function were loaded in on-chip RAM.

An alternative is to provide program code for the Modulation function in external RAM, in order to free up on-chip memory and minimise costs for a single chip DSP. Figure 1 is an example of such an architecture, as used in current Modem application systems. The DSP 1 performs the Datapump function. The program code for the specific Modulation function used during a modem connection exists in external RAM 2. A slow external memory 3 stores the program code for the whole modem application. This slow external memory 3 is usually a FLASH memory, and is provided as a feature for code-version upgradability. Depending on the Modulation function used, the program code for the Datapump function is loaded into external RAM 2. The memory requirements of this Modulation function code is high because the entire code corresponding to this function is loaded. A significant problem associated with the architecture of Figure 1 is that execution of the modulation function is slowed, as compared to an on-chip DSP RAM architecture, due to the external RAM being generally slower and interfacing delays between the DSP chip and the external RAM.

## OBJECT OF THE INVENTION

It is an object of the invention to provide an architecture and data transfer method to reduce on-chip RAM requirements in a DSP particularly, but not exclusively, in a modem whilst maintaining efficiency.

## SUMMARY OF THE INVENTION

In accord with the object of the invention a modem architecture is presented which significantly reduces on-chip RAM requirements. The Downloadable architecture proposed subdivides the Modulation function into phases separated by inactivity intervals. The program code segments corresponding to these phases are dynamically downloaded to on-chip RAM during the inactivity intervals without affecting the performance of the modem.

In particular, one aspect of the invention provides a method of data transfer for use with a signal processor, including:

establishing a program code for executing a data transfer function, the function being divided into phases by inactivity intervals, and the program code including code segments associated with each phase; and

downloading each code segment to a memory of the processor prior to commencement of the respective phase for execution thereof.

Preferably, each successively downloaded segment overwrites a previously downloaded segment.

In another aspect, there is provided a modem architecture including:

a signal processor with a first memory;

a second memory external of the signal processor, wherein the second memory is arranged to hold a program code divided into code segments, for executing phases of a modulation function with inactivity intervals therebetween and the first memory is configured

to sequentially receive the segments downloaded from the second memory to a current segment portion of the first memory for executing same; and

an event arbiter for monitoring completion of each phase and requesting a subsequent code segment to be downloaded into the current segment portion, during an associated interval, for execution thereof.

Preferably, the signal processor is a Datapump and the first memory is provided as on-chip RAM of the Datapump.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention is more fully described, by way of non-limiting example only, with reference to the accompanying drawings, in which:

Figure 1 is a diagrammatic representation of a prior art Modem Datapump implementation;

Figure 2 is a diagrammatic representation of a subdivision of a Modulation Function into phases;

Figure 3 is an exemplary diagram of a single chip DSP downloadable architecture, in accordance with the invention; and

Figure 4 is a detailed diagram of the single chip DSP downloadable architecture of Figure 3.

## DETAILED DESCRIPTION OF AN EMBODIMENT OF THE INVENTION

The invention utilises a Modulation function which is subdivided into different phases as shown in Figure 2. These phases are subdivided such that there is an inactivity interval between them. Figure 2 shows the typical phases through which a Modulation function passes

through. The arrowheads 5 indicate the start of the inactivity interval. The program code for executing each phase is likewise separated into code segments (not shown), associated with each respective phase. The code segments are downloaded dynamically depending on the current phase of the Modulation function, to a DSP on-chip RAM of a Modem.

Figure 3 illustrates the proposed single chip DSP Downloadable Modem architecture. It consists of a DSP with on-chip program RAM 6. The different program segments which are to be downloaded into the on-chip RAM are stored in the slow external second memory 7.

Figure 4 presents a detailed view of the proposed Downloadable Modem architecture. A Bootloader 13 which is resident in on-chip ROM, on start-up or reset, loads an Event Arbiter Segment, Down Loader Segment, and Common Modules Segment from slow external memory 14 into the on-chip RAM 12. The initialisations of the modem system are performed by code executing from the Common Modules Segment 10. The Event Arbiter 8 monitors the current phase of the modem connection and on successful completion of the phase, requests the Down Loader 9 to download the program code segment for the next phase from slow external memory 14 into the Current Phase Segment portion 11. The Current Phase Segment code for the next phase is downloaded into on-chip DSP RAM and executed. The sequence of events that occur is further detailed using an example of a modem connection, as follows.

On start-up the Boot-loader 13, loads the modules common to all phases into the Common Modules 10. The initialisation for the modem is then performed. Depending upon the modulation function selected, Phase 1 of that modulation function is downloaded from slow external memory 14. After successful completion of Phase 1, the Event Arbiter 8 requests the Down Loader 9 to download Phase 2 from external memory into 14 the Current Phase Segment portion 11. The copied code corresponding to Phase 2 of the Datapump function overlays the existing code corresponding to Phase 1 of the Datapump function. The download operation takes place during the inactivity interval which exists between the termination of Phase 1 and the commencement of Phase 2. Phase 2 is then executed. After successful

completion of Phase 2 the Event Arbiter 8 requests the Down Loader 9 to download Phase 3 from slow external memory 14 into the Current Phase segment 11. The Current Phase Segment 11 thus has Phase 2 replaced by Phase 3. The download operation takes place during the inactivity interval which exists between the termination of Phase 2 and the commencement of Phase 3. The program for Phase 3 is then executed. This methodology is followed for the subsequent Phases of the Datapump function.

The total on-chip RAM 12 requirements includes that which is required by the Event Arbiter 8, Down Loader 9, Common Modules 10 and the Current Phase Segment 11. The memory requirements for the Current Phase Segment portion 11 is the maximum of the memory requirements of the individual phases. Thus subdivision of the Modulation Function into phases and overlaying of the code corresponding to the different Phases leads to a substantial reduction in on-chip RAM requirements in single chip DSP downloadable modem architectures.

This procedure easily incorporates inclusion of other applications by modifying the Event Arbiter 8. The new application can be loaded into the Current Phase Segment 11 when necessary. Hence a provision for integration of multiple applications which can be non-concurrently executed by the DSP is provided by this scheme. This ease in integration increases the DSP on-chip RAM requirements marginally by following the code overlay procedure for these multiple applications.

The mandatory requirement for this code overlay procedure which leads to a substantial decrease in DSP on-chip memory is the existence of inactivity intervals. Also the time required for the largest program code download should be within the duration of the inactivity intervals. Hence appropriate external slow memories which meet the latency requirements should be selected. This is exemplified by the equations given below.

The memory size of the Current Phase Segment 10 $S_{max}$ is given by

$S_{max} = \max (S_i)$

where,

$S_i$ is the size of the $i^{th}$ Phase in words

The following inequality should be satisfied;

$(T_{Acc\_int} + T_{Acc\_ext} + T_{Inst\_exec}) * S_i + T_{Margin} \leq T_i$

where,

$T_{Acc\_ext}$ is the slow external memory access time

$T_{Acc\_int}$ is the on-chip RAM access time

$T_{Inst\_exec}$ is the DSP instructions execution overhead for each word transfer

$T_{Margin}$ is the overhead for executing the Down Loader

$T_i$ is the inactivity interval for the $i^{th}$ Phase

This invention outlines a downloadable implementation for modem architectures which are amenable for implementation of these download procedures. Hence it is possible to achieve significant reduction in the DSP on-chip memory requirements.

The present invention provides a significant reduction in cost for single chip DSP solutions for downloadable modem applications. It outlines the procedures for downloadable implementation of the low cost single chip DSP solutions for modem applications. It also provides easy downloadability for other applications which can be executed by the DSP non-concurrently.

The above modem architecture and method has been described by way of non-limiting example only and many modifications and variations may be made thereto without departing from the spirit and scope of the invention.

THE CLAIMS:

1. A method of data transfer for use with a signal processor, including:

establishing a program code for executing a data transfer function, the function being divided into phases by inactivity intervals, and the program code including code segments associated with each phase; and

downloading each code segment to a memory of the processor prior to commencement of the respective phase for execution thereof.

2. A method as claimed in claim 1, wherein each successively downloaded segment overwrites a previously downloaded segment.

3. A method as claimed in claim 1 or 2, wherein the data transfer function is a modem modulation function.

4. A method as claimed in any one of claims 1 to 3, wherein the program code is held in a second memory, external of the signal processor.

5. A method as claimed in any one of claims 1 to 4, wherein the signal processor is in the form of a Datapump.

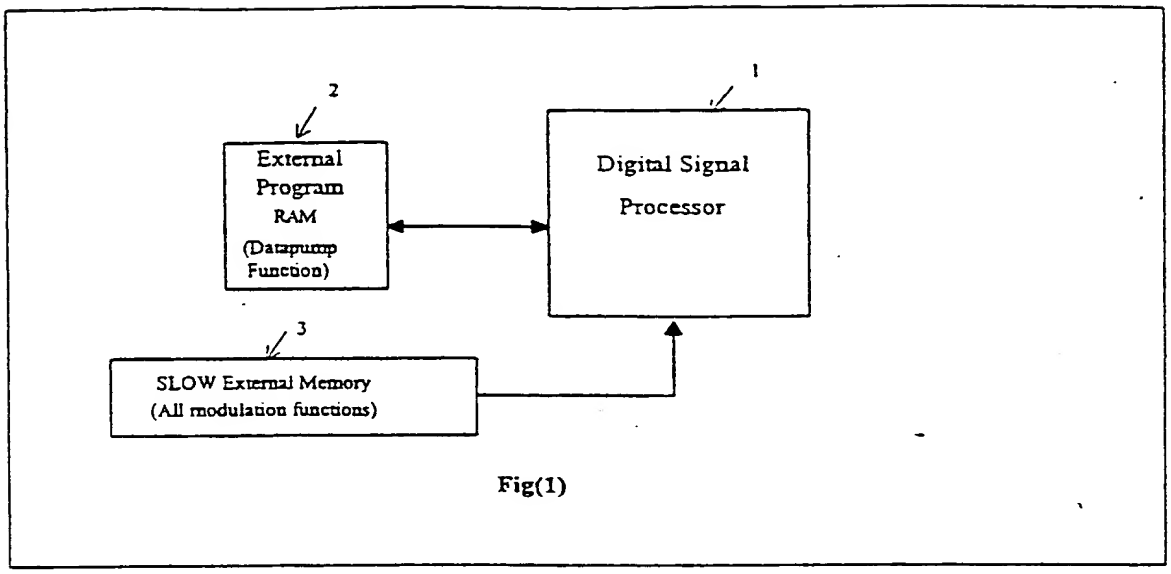
6. A modem architecture including:

a signal processor with a first internal memory;

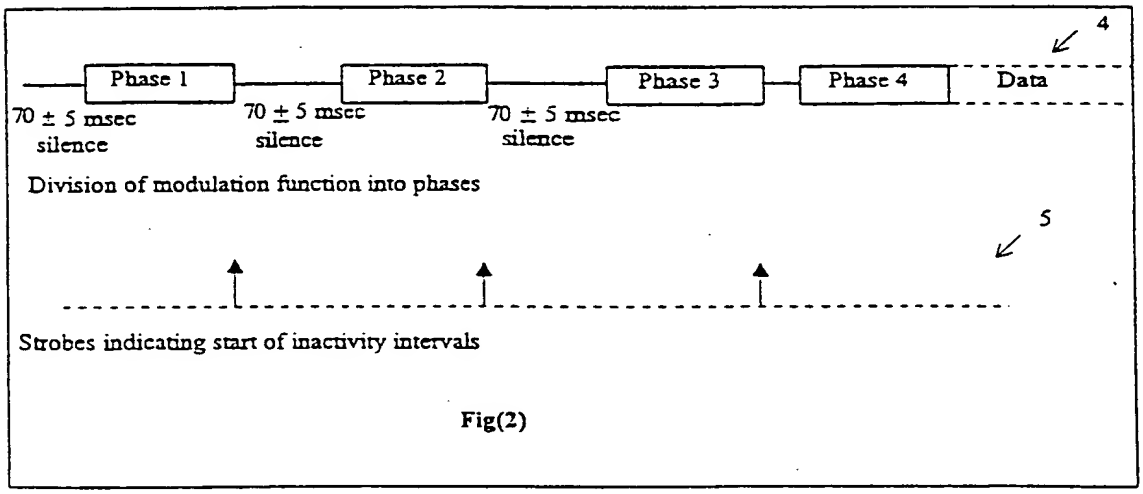
a second memory external of the signal processor, wherein the second memory is arranged to hold a program code divided into code segments, for executing phases of a modulation function with inactivity intervals therebetween and the first memory is configured to sequentially receive the segments downloaded from the second memory to a current segment portion of the first memory for executing same;

an event arbiter for monitoring completion of each phase and requesting a subsequent code segment to be downloaded into the current segment portion, during an associated interval, for execution thereof.

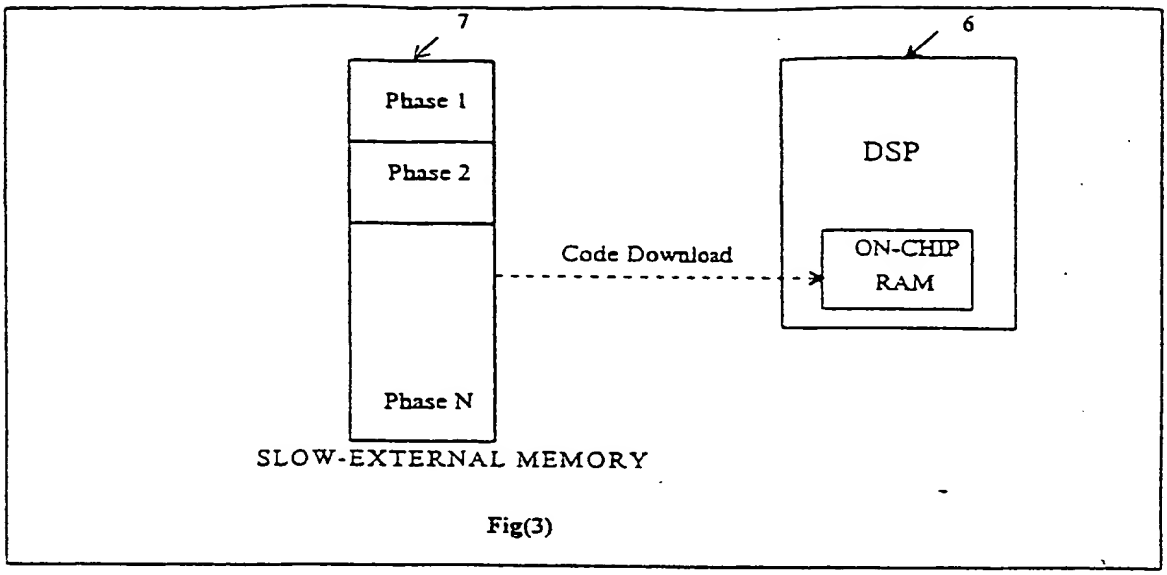
7. A modem architecture as claimed in claim 6, wherein the signal processor is a Datapump and the first memory is provided as on-chip RAM of the Datapump.


2
1
External Program RAM (Datapump Function)
Digital Signal Processor
3
SLOW External Memory (All modulation functions)

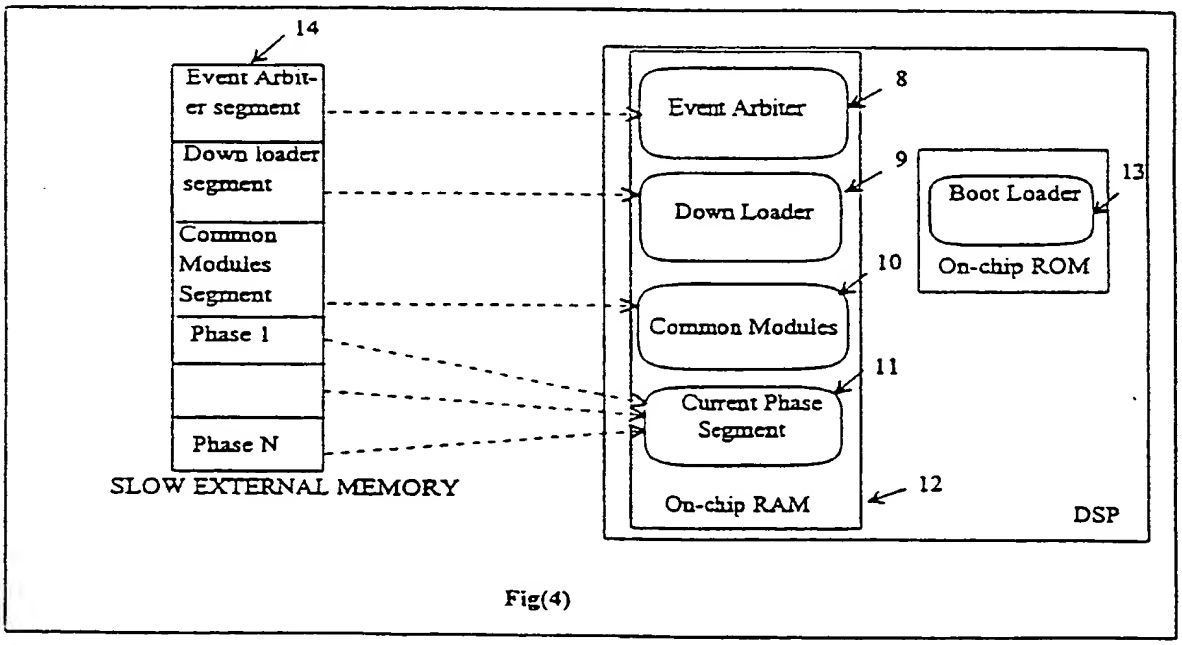
Fig(1)


4
Phase 1
Phase 2
Phase 3
Phase 4
Data
70 ± 5 msec silence
70 ± 5 msec silence
70 ± 5 msec silence
Division of modulation function into phases
5
Strobes indicating start of inactivity intervals

Fig(2)


7
6
Phase 1
Phase 2
Phase N
DSP
ON-CHIP RAM
Code Download
SLOW-EXTERNAL MEMORY

Fig(3)


14
Event Arbit-er segment
Down loader segment
Common Modules Segment
Phase 1
Phase N
SLOW EXTERNAL MEMORY
Event Arbiter
8
Down Loader
9
Common Modules
10
Current Phase Segment
11
On-chip RAM
12
Boot Loader
13
On-chip ROM
DSP

Fig(4)

# INTERNATIONAL SEARCH REPORT

International Application No
PCT/SG 98/00086

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F9/445 H04M11/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F H04M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | WILSON HO W ET AL: "AN APPROACH TO GENUINE DYNAMIC LINKING" SOFTWARE PRACTICE & EXPERIENCE, vol. 21, no. 4, 1 April 1991, pages 375-390, XP000147180 | 1-7 |
| Y | see page 380, line 1 - line 40; figure 2 | 6,7 |
| A | EP 0 772 370 A (IBM) 7 May 1997 | 1,3-5 |
| Y | see column 6, line 7 - line 47; figures 2,3 | 6,7 |

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 18 June 1999 | 25/06/1999 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Kingma, Y |

1

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/SG 98/00086

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| EP 0772370 A | 07-05-1997 | JP 9134320 A | 20-05-1997 |

DSP based systems perform numerical operations on data and are optimised for such operations. A bottleneck in extracting the maximum performance is the limitation imposed by access times to memory. This is usually circumvented by providing on-chip RAM/ROM to supplement the basic DSP core. ROM based solutions preclude upgradability. Downloadable Modem architectures employ on-chip RAM for easy upgradability. This on-chip RAM is expensive compared to slower external memories like SDRAM, Flash etc.

A typical Datapump function has significant internal memory requirements. A straightforward implementation leads to an expensive single chip solution for Downloadable Modem architectures. This implies a large on-chip RAM requirement if all the program code corresponding to the Handshake and Data phase of the Modulation function were loaded in on-chip RAM.

An alternative is to provide program code for the Modulation function in external RAM, in order to free up on-chip memory and minimise costs for a single chip DSP. Figure 1 is an example of such an architecture, as used in current Modem application systems. The DSP 1 performs the Datapump function. The program code for the specific Modulation function used during a modem connection exists in external RAM 2. A slow external memory 3 stores the program code for the whole modem application. This slow external memory 3 is usually a FLASH memory, and is provided as a feature for code-version upgradability. Depending on the Modulation function used, the program code for the Datapump function is loaded into external RAM 2. The memory requirements of this Modulation function code is high because the entire code corresponding to this function is loaded. A significant problem associated with the architecture of Figure 1 is that execution of the modulation function is slowed, as compared to an on-chip DSP RAM architecture, due to the external RAM being generally slower and interfacing delays between the DSP chip and the external RAM.

OBJECT OF THE INVENTION

It is an object of the invention to provide an architecture and data transfer method to reduce on-chip RAM requirements in a DSP particularly, but not exclusively, in a modem whilst maintaining efficiency.

SUMMARY OF THE INVENTION

In accord with the object of the invention a modem architecture is presented which significantly reduces on-chip RAM requirements. The Downloadable architecture proposed subdivides the Modulation function into phases separated by inactivity intervals. The program code segments corresponding to these phases are dynamically downloaded to on-chip RAM during the inactivity intervals without affecting the performance of the modem.

In particular, one aspect of the invention provides a method of data transfer for use with a signal processor, including:

establishing a program code for executing a data transfer function, the function being divided into phases by inactivity intervals, and the program code including code segments associated with each phase; and

downloading each code segment to a memory of the processor prior to commencement of the respective phase for execution thereof.

Preferably, each successively downloaded segment overwrites a previously downloaded segment.

In another aspect, there is provided a modem architecture including:

a signal processor with a first memory;

a second memory external of the signal processor, wherein the second memory is arranged to hold a program code divided into code segments, for executing phases of a modulation function with inactivity intervals therebetween and the first memory is configured

to sequentially receive the segments downloaded from the second memory to a current segment portion of the first memory for executing same; and

an event arbiter for monitoring completion of each phase and requesting a subsequent code segment to be downloaded into the current segment portion, during an associated interval, for execution thereof.

Preferably, the signal processor is a Datapump and the first memory is provided as on-chip RAM of the Datapump.

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The invention is more fully described, by way of non-limiting example only, with reference to the accompanying drawings, in which:

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Figure 3 is an exemplary diagram of a single chip DSP downloadable architecture, in accordance with the invention; and

Figure 4 is a detailed diagram of the single chip DSP downloadable architecture of Figure 3.

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2. A method as claimed in claim 1, wherein each successively downloaded segment overwrites a previously downloaded segment.

3. A method as claimed in claim 1 or 2, wherein the data transfer function is a modem modulation function.

4. A method as claimed in any one of claims 1 to 3, wherein the program code is held in a second memory, external of the signal processor.

5. A method as claimed in any one of claims 1 to 4, wherein the signal processor is in the form of a Datapump.

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